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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,306	03/07/2002	Hiroyuki Fujiyama	1614.1225	8386

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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	5

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,306	FUJIYAMA, HIROYUKI	
	Examiner	Art Unit	
	Bao Q Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-12* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The examiner acknowledges the applicant's submission of the amendment dated on 01 March 2004. At this point, claims 1, 5, and 8 have been amended; claims 11 and 12 have been added. Thus, claims 1-12 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5-6, 8-9, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Mittal et al. (U.S. Patent No. 5,889,983).

Referring to claim 1, Mittal discloses a circuit comprising:

a register which stores therein a semaphore address as a process-compare-operand (PCO) register stores a source operand "**SRC2**" specifying an address location where the reference lock or semaphore value is stored (see figure 6: element 64, column 3: lines 11-22, column 5: lines 45-51, and column 8: lines 32-44); and

a semaphore control circuit which asserts a control signal in response to a read access by a processor directed to the semaphore address, and negates the control signal in response to a write access by the processor directed to the semaphore address as a bus interface unit (see figure 6: element 54b) setting a lock state for a shared space in the read phase of an atomic read-modify-write operation to the shared space (see column 4: lines 33-47, column 8: lines 65-67,

and column 9: lines 1-4) and resetting the lock state for the shared space in the write phase of the atomic read-modify-write operation to the shared space (see column 4: lines 33-47, and column 9: lines 13-27),

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted as if the reference lock is set for the shared space by a processor, other processors are not allowed to access the shared space (see column 4: lines 38-47).

As to claim 2, Mittal further discloses that the circuit comprising a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match as an execution unit executes a compare-and-exchange instruction to compare source operand **SRC2** with source operand **SRC1** specified by the instruction (see column 8: lines 50-67), a signal indicating a match or a true value of comparison is inherently existing; wherein said semaphore control circuit includes:

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from the processor as a bus interface unit (see figure 6: element 54b) setting a lock state in the read phase of an atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4); and

a circuit which sets the control signal to a negated state in response to assertion of the match signal and an indication of a write operation by a read/write signal output from the processor as a bus interface unit (see figure 6: element 54b) resetting the lock state in the write

phase of the atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, and column 9: lines 13-27).

Referring to claim 5, Mittal discloses a processor comprising:

a processor core (see figure 6: element 50b);

a register which stores therein a semaphore address as a process-compare-operand (PCO) register stores a source operand "**SRC2**" specifying an address location where the reference lock or semaphore value is stored (see figure 6: element 64, column 3: lines 11-22, column 5: lines 45-51, and column 8: lines 32-44); and

a control circuit which asserts a control signal in response to a read access by said processor core directed to the semaphore address, and negates the control signal in response to a write access by said processor core directed to the semaphore address as a bus interface unit (see figure 6: element 54b) setting a lock state for a shared space in the read phase of an atomic read-modify-write operation to the shared space (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4) and resetting the lock state for the shared space in the write phase of the atomic read-modify-write operation to the shared space (see column 4: lines 33-47, and column 9: lines 13-27),

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted as if the reference lock is set for the shared space by a processor, other processors are not allowed to access the shared space (see column 4: lines 38-47).

As to claim 6, Mittal further discloses that said control circuit includes:

a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match as an execution unit executes a compare-and-exchange instruction to compare source operand **SRC2** with source operand **SRC1** specified by the instruction (see column 8: lines 50-67), a signal indicating a match or a true value of comparison is inherently existing;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from the processor core as a bus interface unit (see figure 6: element 54b) setting a lock state in the read phase of an atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4); and

a circuit which sets the control signal to a negated state in response to assertion of the match signal and an indication of a write operation by a read/write signal output from the processor core as a bus interface unit (see figure 6: element 54b) resetting the lock state in the write phase of the atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, and column 9: lines 13-27).

Referring to claim 8, Mittal discloses a multi-processor system, comprising:

a plurality of processors (see figure 1, column 1: lines 5-9, and column 9: lines 36-41);

a memory shared by said plurality of processors (see figure 6: element 15); and

a semaphore register for controlling exclusive use of said memory as a register in the system memory stores the reference lock or semaphore value controlling exclusive use of shared memory (see figure 6: element 64, column 3: lines 11-22, column 5: lines 45-51, and column 8: lines 32-44), wherein at least one of said plurality of processors include:

a processor core (see figure 6: element 50b);

an address register which stores therein an address of said semaphore register as a process-compare-operand (PCO) register stores a source operand "**SRC2**" specifying an address location where the reference lock or semaphore value is stored (see figure 6: element 64, column 3: lines 11-22, column 5: lines 45-51, and column 8: lines 32-44); and

a control circuit which asserts a control signal in response to a read access by said processor core directed to the semaphore address, and negates the control signal in response to a write access by said processor core directed to the semaphore address as a bus interface unit (see figure 6: element 54b) setting a lock state for a shared space in the read phase of an atomic read-modify-write operation to the shared space (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4) and resetting the lock state for the shared space in the write phase of the atomic read-modify-write operation to the shared space (see column 4: lines 33-47, and column 9: lines 13-27),

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted as if the reference lock is set for the shared space by a processor, other processors are not allowed to access the shared space (see column 4: lines 38-47).

As to claim 9, Mittal further discloses that said control circuit includes:

a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match as an execution unit executes a compare-and-exchange instruction to compare source operand **SRC2** with source operand **SRC1** specified by the instruction (see column 8: lines 50-67), a signal indicating a match or a true value of comparison is inherently existing;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from the processor core as a bus interface unit (see figure 6: element 54b) setting a lock state in the read phase of an atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4); and

a circuit which sets the control signal to a negated state in response to assertion of the match signal and an indication of a write operation by a read/write signal output from the processor core as a bus interface unit (see figure 6: element 54b) resetting the lock state in the write phase of the atomic read-modify-write operation if the comparison value is true (see column 4: lines 33-47, and column 9: lines 13-27).

Referring to claim 11, Mittal teaches a method for controlling a semaphore in a system including at least one processor, comprising:

asserting a control signal when the processor performs a read access to the semaphore address as setting a lock state for a shared space in the read phase of an atomic read-modify-write operation to the shared space (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4); and

negating the control signal when the processor performs a write access to the semaphore address as resetting the lock state for the shared space in the write phase of the atomic read-modify-write operation to the shared space (see column 4: lines 33-47, and column 9: lines 13-27).

Referring to claim 12, Mittal discloses a circuit, comprising

a register which stores therein a semaphore address as a process-compare-operand (PCO) register stores a source operand "**SRC2**" specifying an address location where the reference lock or semaphore value is stored (see figure 6: element 64, column 3: lines 11-22, column 5: lines 45-51, and column 8: lines 32-44); and

a semaphore control circuit which asserts a control signal in response to a read access by a processor directed to the semaphore address, and negates the control signal in response to a write access by the processor directed to the semaphore address as a bus interface unit (see figure 6: element 54b) setting a lock state for a shared space in the read phase of an atomic read-modify-write operation to the shared space (see column 4: lines 33-47, column 8: lines 65-67, and column 9: lines 1-4) and resetting the lock state for the shared space in the write phase of the

atomic read-modify-write operation to the shared space (see column 4: lines 33-47, and column 9: lines 13-27), the control signal preventing other processors from accessing the semaphore address as if the reference lock is set for the shared space by a processor, other processors are not allowed to access the shared space (see column 4: lines 38-47).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mittal et al. (U.S. Patent No. 5,889,983) in view of Capps Jr. et al. (U.S. Patent No. 5,430,860).

As to claim 3, 7, and 10, Mittal discloses all the limitation as respectively discussed in claim 1,5, and 8. However, Mitten does not clearly discloses that a right to use a bus given to the processor is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal.

Capps Jr. discloses a system to manage atomic operation similar to that of Mittal. Capps Jr. further discloses that a right to use a bus given to the processor is not relinquished in response

to a bus-arbitration request supplied from an external source during an asserted state of the control signal (see Abstract, column 2: lines 53-67, and column 3: lines 1-28 of Capps Jr.).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify Mittal's system so that the right to use a bus given to the processor is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal. This would have been obvious because an atomic operation is required to be completed without interruption once the operation begins to execute (see column 2: lines 31-33 of Mittal; and Abstract of Capps Jr.). By assuring that a right to use a bus given to the processor is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal, the integrity of semaphore data is not compromised by premature release of the lock signal (see column 3: lines 11-20 of Capps Jr.) and the atomic nature of atomic operation is assured.

Response to Arguments

6. Applicant's arguments filed on 01 March 2004 have been fully considered but they are not persuasive.

The applicant argues on page 7 that "elements 54b in Mittal does not teach or suggest asserting a control signal in response to a read access by a processor, nor negating the control signal in response to a write access by the processor". The examiner disagrees and directs the applicant's attention to column 6: lines 22-29 of Mittal where an agent (processor) performs a read-modify-write operation to a shared memory space. During the read phase, the agent obtains a lock on the shared memory space by setting a lock state (see column 4: lines 33-47, column 8:

lines 65-67, and column 9: lines 1-4); and during the write phase, the agent releases the lock on the shared memory space by resetting the lock state (see column 4: lines 33-47, and column 9: lines 13-27). Furthermore, Mittal discloses that when the reference lock is set for the shared memory space by a processor, other processors are not allowed to access the shared space (see column 4: lines 38-47). Clearly, claims 1-2, 5-6, 8-9, and 11-12 are anticipated by Mittal.

Allowable Subject Matter

7. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **three months** from the mailing date of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUE TRUONG

BT

Patent Examiner

20 April 2004

Donald A. Sparks

Supervisory Patent Examiner

Technology Center 2100